Amendments to the Specification:

On page 19, please replace the two paragraphs beginning at line 11 and ending with line 34 with the following two amended paragraphs:

Space compactors, 217 to 219, are used to reduce the number of bit streams in test responses, 110, 113, 116, and 119 shifted out of CD1 102, CD2 103, CD3 104, and CD4 105, respectively. Space compactors are optional and are only used when the overhead of a MISR becomes a concern. The outputs of the space compactors are then compressed by multiple input signature registers (MISRs), 220 to 222. The contents of MISRs after all test stimuli are applied become signatures, 236 to 238. The signatures are then be compared by comparators, 223 to 225, with corresponding expected values. The error indicator 226 is used to combine the individual pass/fail signals, 242 to 244, a global pass/fail signal 245. Alternatively, the signatures in MISRs 220 to 222 can be shifted to the outside of the design for comparison through a single scan chain composed of elements 223, 239, 224, 240, 225, and 241.

The central self-test controller 202 controls the whole test process by manipulating individual scan enable signals, 204 to 207, and by reconfiguring capture clocks, CK1 111 to CK4 120. Especially, the scan enable signals, 204 to 207, can be controlled by one global scan enable signal GSE 201, which can be a slow signal in that it does not have to settle down in half of the cycle of any clock applied to any clock domain. Some additional control

signals 203, connected to 208, 209 and 210, are needed to conduct other control tasks.

On Page 20, please replace the paragraph beginning at line 7 with the following amended paragraph:

All storage elements in PRPGs, 211 to 213, and MISRs, 220 to 222, can be connected into a scan chain through paths 246 to 252 from which predetermined patterns can be shifted in for reseeding and computed signatures can be shifted out for analysis. This configuration helps in increasing fault coverage and in facilitating fault diagnosis.

On page 24, please replace the paragraph beginning at line 7 with the following amended paragraph:

FIG. 6 shows a timing diagram of a feed-forward partial-scan design given in FIG. 1, of one embodiment of the invention for detecting or locating stuck-at faults within each clock domain and stuck-at faults crossing clock domains with a shortened yet ordered sequence of capture clocks in self-test or scan-test mode. It is assumed that the clock domains CD1 102 to CD4 105 contain a number of un-scanned storage cells that form a sequential depth of no more than 2. The timing diagram [[600]] shows the sequence of waveforms of the 4 capture clocks, CK1 111 to CK4 120, operating at the same frequency.

On page 24, please replace the paragraph beginning at line 22 with the following amended paragraph:

During each capture cycle 607 which extends through the intervals 601 to 605, two sets of capture clock pulses are applied in the following order: First, three pulses of 10MHz, two being functional pulses and one being a capture pulse, are applied to CK1 111 and CK3 117 simultaneously to detect or locate stuck-at faults within the clock domain CD1 102 and CD3 104, respectively. Second, three pulses of 10MHz, two being functional pulses and one being a capture pulse, are applied to CK2 114 and CK4 120 simultaneously to detect or locate stuck-at faults within the clock domain CD2 103 and CD4 105, respectively.

On Page 25, please replace the paragraph beginning at line 8 with the following amended paragraph:

FIG. 7 shows an example full-scan or partial-scan design with a multiple-capture DFT system 701, of one embodiment of the invention. The design 733 is the same as the design 133 given in FIG. 1. Same as in FIG. 1, the 4 clock domains, CD1 702 to CD4 705, are originally designed to run at 150MHz, 100MHz, 100MHz, and 66MHz, respectively. The only difference from FIG. 1 is that these clock frequencies will be used directly without alternation in order to implement at-speed self-test or scan-test for stuck-at, delay, and multiple-cycle delay faults within each clock domain and crossing clock domains. In self-test or scan-test mode, the multiple-capture DFT system 701 will take over the control of all stimuli, 709, 712, 715 and 718, all system clocks, CK1 711 to CK4 720, and all output responses, 710, 713, 716 and 719.